Digital Audio Broadcasting

General–purpose and application–specific design of a DAB channel decoder

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In 1988, the first public demonstrations of a new Digital Audio Broadcasting system were given in Geneva. Although this showed the feasibility of digital compression and modulation for digital radio, a lot of work remained to be done in the fields of standardization, frequency allocation, promotion and hardware cost and size reduction. This article describes the development of current DAB receivers, with special emphasis on the design of the digital signal processor–based channel decoder which has been used in the 3rd–generation Eureka receivers, as well as a prototype decoder based on an application–specific chip–set.

1. Introduction

Since the introduction of the Compact Disc by Philips in 1982, people have become more and more used to the superior quality and user–friendliness of digital audio. There is every reason, therefore, to arrange for sound broadcasting to benefit also from this trend. Digital Audio Broadcasting (DAB) provides the digital communication link needed to transfer audio signals (already in digital form as they leave modern studios), together with additional services, to the home and mobile receiver without loss of quality. To give an impression of the performance of the DAB system, *Table 1* compares DAB with the Digital Satellite Radio (DSR) system [1] which was introduced in Europe in 1990, and conventional VHF/FM radio extended with the Radio Data System (RDS). Although a DAB receiver is significantly more–complex than a conventional VHF/FM receiver, there are a large number of advantages: CD audio quality, even in a mobile environment [2], operational comfort and numerous possibilities for additional services such as multi–language programmes, paging, continuous weather and traffic information and audio–visual advertising.

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Parameters	Systems		
	VHF/FM + RDS	**DSR**	**DAB**
Transmission	Terrestrial	Satellite	Satellite & Terrestrial
Reception	Home / Mobile	Home	Home / Mobile
RF frequency range	88 – 108 MHz	12 GHz	47 to 230 MHz (*note 1*)
RF sensitivity	≥ 40 dBμV (*note 2*)	≥ 48 dBμV	≥ 24 dBμV
Intermediate frequency	10.7 MHz	118 / 40 MHz	(36 MHz)
Intermediate frequency bandwidth	300 kHz	14 MHz	1.536 MHz
Modulation method	FM + DPSK	Diff. QPSK	OFDM
Multipath resistant	No	No	Yes (allows SFN)
Noise protected	No	Yes	Yes
Number of progs per ensemble	1	16	4 to 16
Audio bandwidth	15 kHz	15 kHz	20 kHz
Audio signal–to–noise ratio (*note 3*)	60 dB	95 dB	> 100 dB
Audio delay	< 1 ms	4 ms	< 500 ms
Audio processing	Analogue	Digital	Digital
Data processing	Digital	Digital	Digital
Data capacity	1.2 kbit/s	11 kbit/s	≥ 32 kbit/s
Error protection	CRC	Block code	Convolutional code
Decoder dissipation (*note 4*)	≤ 200 mW	≤ 500 mW	≤ 2500 mW
Decoder complexity	Low	Medium	High
Year of introduction	1987	1990	1996

Table 1
Comparison of main characteristics of VHF/FM + RDS, DSR and DAB sound broadcasting systems.

Notes: *1* UHF band and 1.5 GHz band possible with DAB Modes II and III
2 FM stereo at 60 dB S/N ratio with high–quality receiver
3 1 kHz sine–wave reference signal
4 Dissipation with 5 V supply, one service selected

Because of world–wide competition, it was important to set a standard in good time, and to be on the market within a few years. In Europe, a DAB standard has now been set within Eureka project 147 [3], in which most of the European consumer electronics companies and many European broadcasting organizations participated. During the finalisation of the standard within Eureka, project AE–14 was initiated within JESSI (Joint European Submicron Silicon Programme), with the aim of making a DAB receiver chip–set with high–level design tools.

Probably within three years from now, these developments will lead to the market introduction of DAB and a car–radio size receiver will be available as an add–on unit for existing car audio equipment. In a later stage, it may be integrated with an FM radio and a Digital Compact Cassette (DCC) player.

2. DAB transmission

2.1. DAB transmitter

A simplified transmiter block diagram is shown in *Fig. 1*. MPEG layer 2 audio coding [4] is used to reduce the linear pulse–code modulation (PCM) audio bit–rate by a factor in the range from 4 to 12, corresponding to audio qualities ranging from CD to normal FM radio. Convolutional coding is applied to add redundancy for error correction at the receiver. For audio applications, unequal error–protection is applied; this means that the code–rate

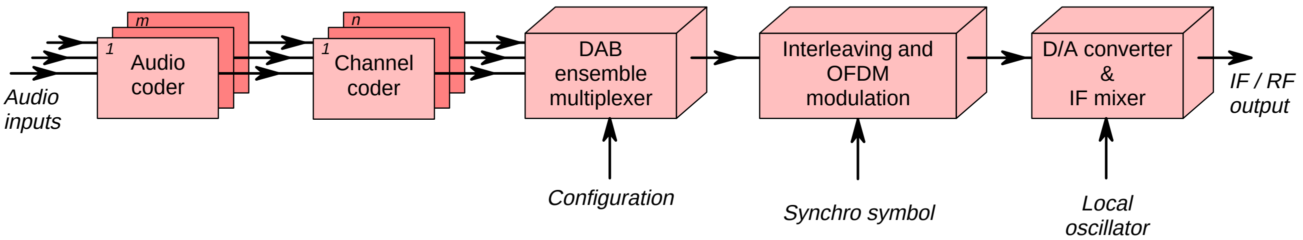


Figure 1
Simplified DAB transmitter block diagram, showing the order of coding, multiplexing and modulation.

After demodulation	After de–interleaving	After error correction
.rirfcFFFrgeltndao	This is aF FxampFe	This is an example
es yr FFFAic cei c	of text cFnFainiFg	of text containing
ernn FFFdueVet hi	error burFtF TotF	error bursts both
sn dr FFF it ner T	in columnF FndTiFT	in columns and in
TTTTTTFFFTTTTTTTTT	lines cauFeF by F	lines caused by
nearFFFdtsa onre	TTannel sFlFctiTF	channel selective
eiefFFFriixrc ui	fading. AFTFr deF	fading. After de–
l ndhqFFFrtb lodml	interTeavFnF in F	interleaving in
vnh FFFc sama ot	time anT FrFquenFy	time and frequency
yrtoezFFFeec nimtf	theTe errFrFThavF	these errors have
geianvFFFnateeea i	been randFmFzed Fs	been randomized as
rniitFFFah.grseat	indiTaTedF FfterF	indicated. After
o–eyaFFFseuiott b	error corFeFtionF	error correction
emoiFFFrdni nr b	by a VitTFbF de–F	by a Viterbi de–
n ennFFFvbl ient	coder theFoFiginFl	coder the original
rpoixFFFudarbedee	teTt is rFcFvereF.	text is recovered.

Figure 2
Illustration of the effect of de–interleaving in association with error correction in the decoder.

varies step–wise within a frame [5]. This is applicable in the case of audio signal transmissions because the significance of the bits within a frame is different, in contrast to the situation for data transmission applications where each bit is equally important.

The encoded bit–stream is then interleaved in time as well as in frequency [6]. Time interleaving is used to spread out, over a long period of time, the rapid channel variations that occur in mobile reception. Even if the baseband signal drops out completely for a brief period, enough information may remain in each frame to permit reconstruction of the original source sequence. This process is illustrated in *Fig. 2*, which shows a text in which the lines correspond to time frames and the columns to frequency bands. Errors caused by frequency–selective fading are indicated by **F** and errors due to time fading are indicated by ***T***. After de–interleaving in the receiver, the missing characters are dispersed and error correction is possible because of the redundancy within the text; this would not have been possible without interleaving because several consecutive characters would have been missing.

The transmission equipment includes a multiplexer which builds a DAB "ensemble" from several audio and data streams, having different bit–rates and code–rates. Information about the ensemble is inserted into the data–stream for service selection (demultiplexing) in the receiver.

For modulation, the orthogonal frequency–division multiplex (OFDM) technique is used [7, 8]. Instead of using one wide–band carrier with the data changing at a high rate, multiple narrow–band carriers are used, on each of which the data changes at a much lower rate. This significantly reduces the amount of inter–symbol interference (ISI) resulting from a fading mobile channel [9].

Interleaving in the frequency domain is obtained by re–arranging the carrier order within a symbol, according to a fixed scheme. This will cause the frequency–selective fading that occurs in reception to be spread out across the full transmission bandwidth.

After digital–to–analogue conversion, the data are modulated in quadrature onto a radio–frequency signal. This means that the transmitted DAB signal is the sum of two RF signals of the same frequency and having a mutual phase shift of 90°. These signals are modulated with an in–phase (I) and a quadrature (Q) component of the baseband signal.

2.2. Baseband signal

The complex baseband signal is sub–divided into frames, which contain several services. Every frame consists of a fixed number of symbols, each one composed of a large number of orthogonal carriers with an equal frequency spacing. The bandwidth is 1536 kHz, containing for example 384 carriers with 4 kHz spacing (*Fig. 3*). Every symbol is preceded by a guard interval, in which part of the time signal is cyclicly repeated. As long as the time difference between the first and last reflections occuring in the mobile channel does not exceed the duration of this interval, no ISI will occur and no channel equalization is needed. The reception quality in an urban or hilly area where there are many reflections will be substantially improved compared with other demodulation schemes.

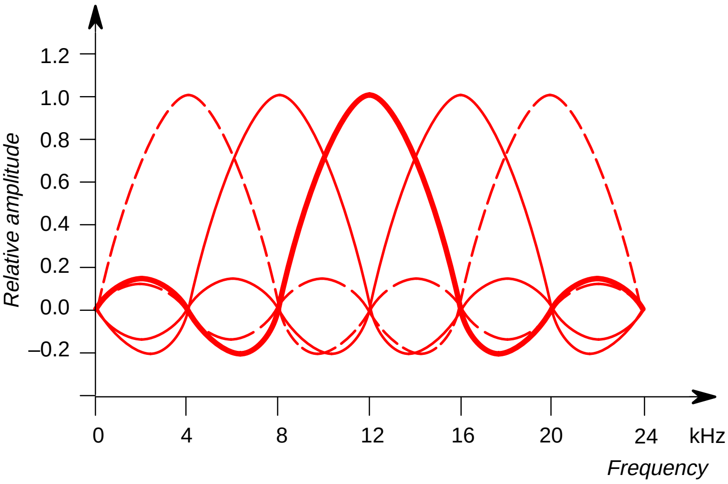


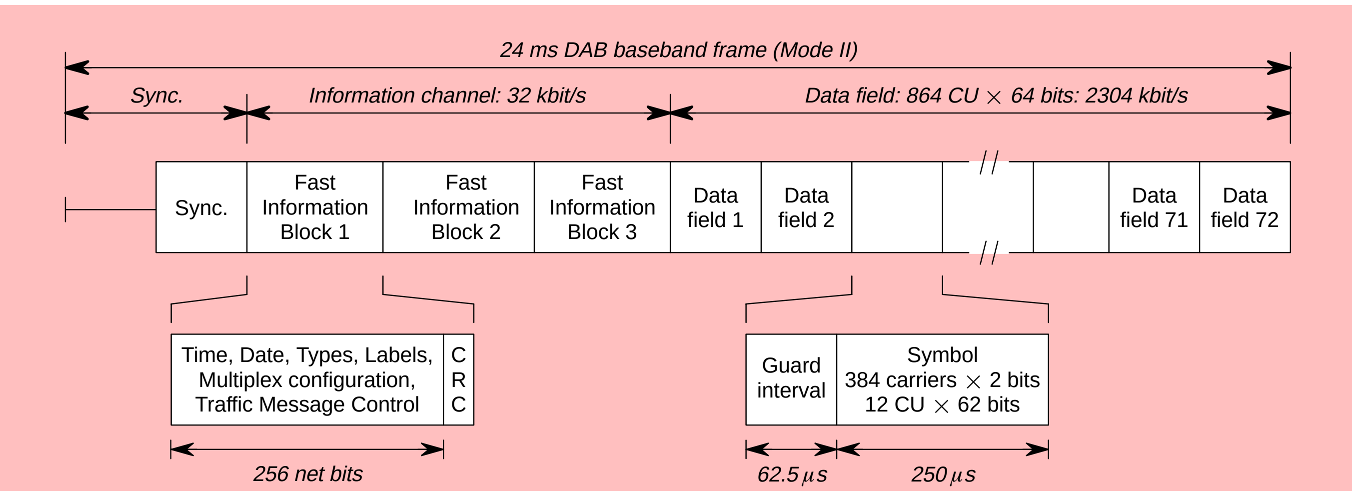
Figure 3
Carrier spectrum showing orthogonality: each carrier has a peak position where all others have zero–crossings.

Parameters	Mode I	Mode II	Mode III
Application	SFN	Terrestrial	Satellite
Frame duration (T_f)	96 ms	24 ms	24 ms
Symbol duration (T_s)	1 ms	250 µs	125 µs
Guard interval (T_g)	246 µs	62 µs	31 µs
No. of symbols/frame (J)	76	76	153
No. of carriers/symbol (N)	1536	384	192
Carrier spacing (f_s)	1 kHz	4 kHz	8 kHz
Bandwidth (f_w)	1536 kHz	1536 kHz	1536 kHz
Max. frequency (f_m)	250 MHz	1 GHz	2 GHz

Table 2
DAB system parameters for Modes I, II and III.

Three operational modes have been defined for different DAB broadcast options. Mode I, which has a long guard interval for the absorption of multi–path reflections, is specially intended for single–frequency networks (SFN), in which several transmitters may share the same band for the same programmes. Modes II and III have a wider carrier spacing to allow higher transmission frequencies to be used without the risk of losing carrier orthogonality at the receiver. An overview of the modes is given in *Table 2*. An example of the frame structure for Mode II is given in *Fig. 4*. The synchro channel (two symbols) is reserved for receiver synchronization. It is followed by the fast information channel (FIC – three symbols) which contains service information such as the multiplex configuration, service labels, paging codes and traffic message control. The data field consists of the remaining symbols and contains data for a variable number of service components in a time multiplex. To simplify service component selection and mode conversion, the data field is sub–divided, in a mode–independent manner, into 864 capacity units (CUs) of 64 gross bits each.

Figure 4
Frame structure of baseband signal in Mode II.



3. Basic functional modules of a DAB receiver.

A functional block diagram of a DAB receiver is given in *Fig. 5*. The channel decoder which handles the digital demodulation and decoding of the baseband signal is indicated within the shaded area. A description of each block is given in this section.

3.1. Front–end

The front–end of a DAB receiver can be derived from a television tuner for bands I and III, corresponding to a frequency range of 50 to 250 MHz. For satellite reception in Modes II or III a 1.5–GHz down–converter is also needed.

In order to maintain carrier orthogonality, it is required that the frequency difference between the transmitter and receiver shall be less than 2.5% of the carrier spacing. For Mode I (SFN) this corresponds to 0.1 ppm at a transmission frequency of 250 MHz. To guarantee adequate selectivity, the IF output signal is passed through a surface acoustic wave (SAW) filter before being applied to the quadrature demodulator.

3.2. Quadrature demodulator

The quadrature demodulator can be realised either in digital form (A/D convertor at the input) or in analogue form (A/D convertor at the output). A quadrature oscillator is used to regenerate the baseband I and Q components, with 768 kHz bandwidth each, from the analogue IF signal. This IF oscillator is adjusted by an automatic frequency control (AFC) signal, which is generated by the synchronization processor.

The SAW filter, together with low–pass filters before the A/D converter(s), provide sideband suppression of about 70 dB. The envelope of the output signal is used for automatic gain control (AGC) and detection of the null symbol which indicates the start of a frame.

3.3. Synchronization processor

After detection of the null symbol, the fast Fourier transform (FFT) of the reference symbol is acquired by the synchronization processor. It is used to calculate the frequency offset of the incoming signal, and delivers an AFC value for the IF oscillator. Frequency offsets as large as ±15 carriers can be detected and adjusted.

Next, the FFT of the reference symbol is correlated with the original reference symbol. Applying an inverse FFT to the result gives the impulse response of the channel.

From analysis of this impulse response, control signals are derived which serve to synchronize the receiver clock generator (voltage–controlled crystal oscillator – VCXO) to the transmitter and to adjust the symbol selection window to avoid interference (removal of the guard interval).

3.4. Demodulation processor

In the receiver, the orthogonal carriers, onto which the data is differentially modulated by quadrature phase–shift keying (QPSK), are derived from the time signal on a symbol basis by means of an FFT. After this FFT the phase difference with respect to the previous symbol is determined for each carrier (*Fig. 6*). Quasi–stationary deviations that occur within the channel as a result of displacement effects are eliminated this way. The reference symbol determines the initial carrier phase value for each frame.

For each carrier, the phase difference is represented as a complex number with two components, called metrics. Each metric separately corresponds to a gross bit, associated with a 3–bit amplitude–dependent reliability indication.

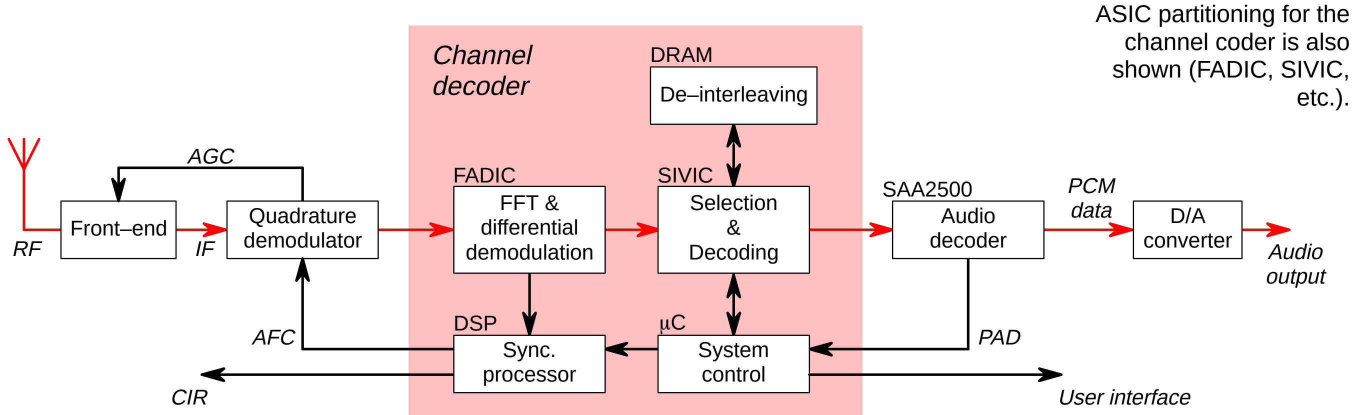


Figure 5
Functional block diagram of a DAB receiver.
ASIC partitioning for the channel coder is also shown (FADIC, SIVIC, etc.).

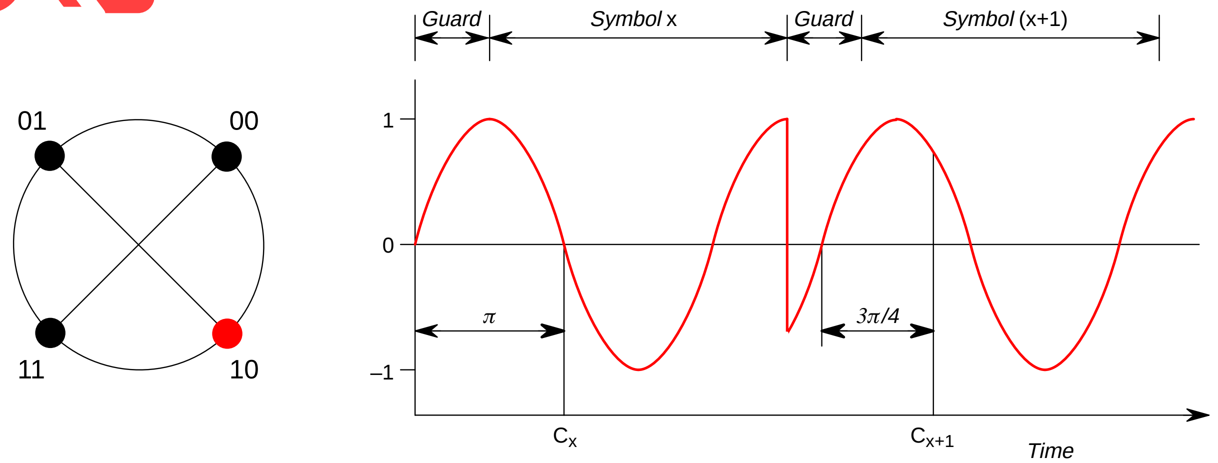


Figure 6
Differential demodulation of one carrier.

The phase difference between successive symbols determines the “di–bit” combination.
In the example shown, $C_{x+1} - C_x = (3\pi/4) - \pi = (-\pi/4)$, corresponding to a “10” bit combination.

3.5. Decoder

Error bursts caused by fluctuations in the mobile channel are pseudo–randomly distributed by de–interleaving in the receiver. Since this operations is complementary to the interleaving in the transmitter, the output sequence is equal to the input sequence, but with a delay of 15 frames. About 2 kbits of memory is needed for the de–interleaving of one capacity unit (CU).

The de–interleaving process removes undesired metric correlation at the input of a Viterbi decoder which serves for error correction [9]. The Viterbi decoder uses redundancy added at the encoder to reconstruct the originally transmitted sequence with maximum likelihood. Soft–decision logic is used, which means that it takes into account the reliability indication available from each metric.

The amount of redundancy added at the encoder may be different for each programme or each application, and it should be matched to the channel characteristics. This is obtained by puncturing the coded bit–stream according to a known scheme. For cable distribution a significantly smaller amount of redundancy is needed compared to that for wireless communication in a hilly terrain. For data applications one can choose a code rate *R* (ratio between net bits and gross bits) of 1/4, 3/8, 1/2 or 3/4.

3.6. Audio decoder

The audio decoder takes the compressed source signal as its input and performs an inverse quantizing operation on 32 equally–spaced audio subbands, to obtain a PCM digital audio signal with full 20–bit accuracy. The operation is based upon the psychoacoustic properties of the human ear, which masks weak frequencies delivered simultaneously with loud frequencies. Depending on the required audio quality, the input bit–stream is fixed from 32 kbit/s (speech, mono) to 384 kbit/s (studio quality, stereo). A programme–associated data stream (PAD) may be included in the audio bit–stream; this could contain, for example the Interactive Text Transmission System (ITTS) giving information such as artists’ names, titles or lyrics.

3.7. System control

The receiver should first select a DAB ensemble and then a service within it. A service may contain any combination of audio and data components. Information is provided to select a service by either number, name or type. Since the amount of service information within DAB is almost unlimited, the user will have to make a choice between the facilities offered. A display will present ensemble and service information [10].

Service selection by the user will be processed by a micro–controller, which first interrogates the fast information channel (FIC) to find out where the selected service components are allocated in the data field. A cyclic redundancy check is performed to check the validity of the FIC data. If it is valid, the information is transferred to the decoder which extracts and processes the service components. The PAD data will be passed back to the micro–controller for display. To reduce the demands on processing capability and power dissipation, the receiver will not process service components which are not selected.

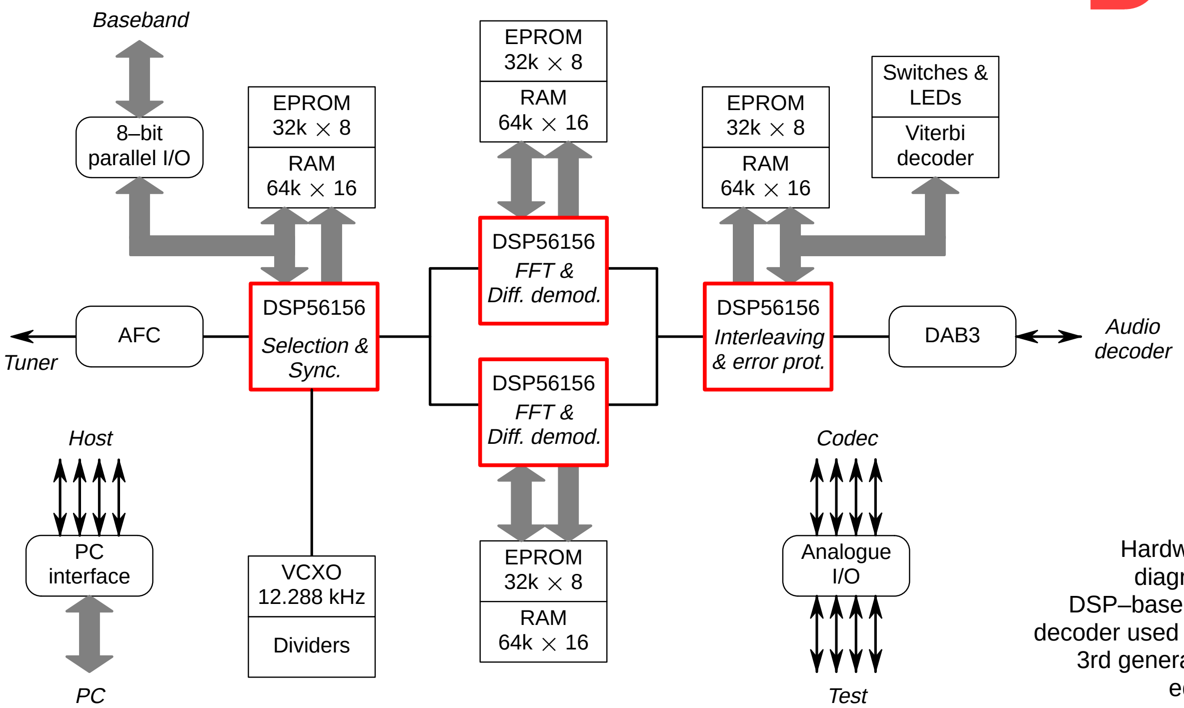


Figure 7
Hardware block diagram of the DSP–based channel decoder used in Eureka 3rd generation DAB equipment.

4. DAB receiver prototypes

4.1. DSP–based prototype implementation

The development of a prototype channel encoder/decoder took place in parallel with standardization within EUREKA–147. Although the basic functionality was known and verified at the start of this hardware development, the DAB system parameters were still changing and the overall system complexity was gradually increasing. Therefore a channel decoder was designed which was based upon a general–purpose multi–processor architecture; this approach provided maximum flexibility, required minimum glue logic and uses a single programming language. Four digital signal processors (DSP) were used (DSP56156), each one having two identical serial interfaces allowing communication in either a serial, parallel or ring configuration. For the implementation of the audio decoder one DSP56001 was used, this having the 24–bit precision required for audio channels [11].

A block diagram of the channel decoder DSP board is depicted in *Fig. 7* and the printed–circuit board (PCB) is shown in *Fig.8*. The functionality of each major system block, based upon the processor capability, is roughly indicated in this diagram. Since the DSPs are too slow to do a real–time FFT on a symbol basis, the symbols associated with the selected service component are stored and processed on a double–frame basis. A separate memory–mapped Viterbi decoder is needed since the DSPs do not have the performance needed for this function.

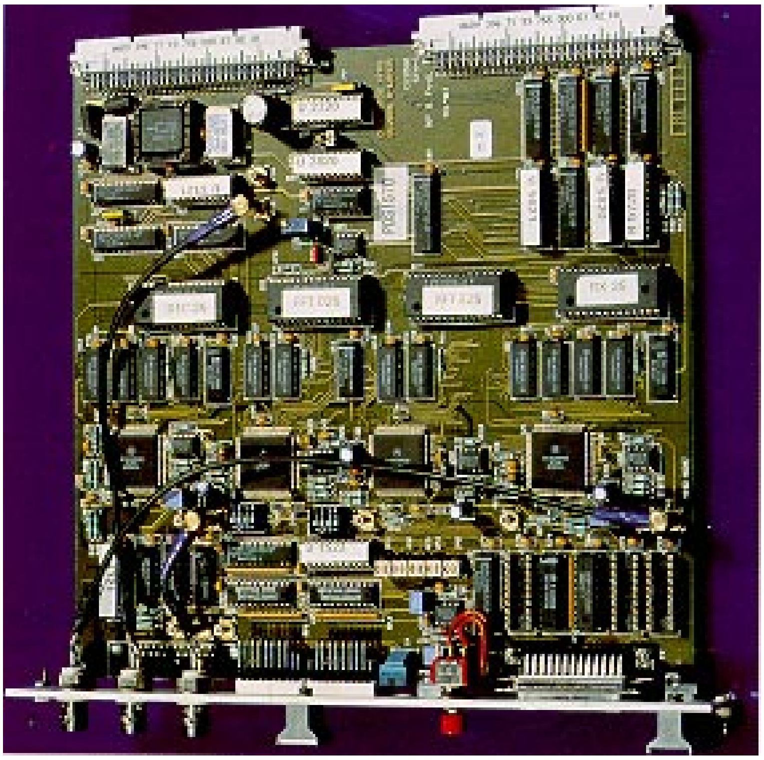


Figure 8
DSP–based Philips channel decoder board used in Eureka 3rd generation equipment.

All DAB–specific interfaces as well as the DSP address decoders and clock dividers are implemented with simple gate–array logic (GAL) devices (type 16V8). This allowed the correction of mistakes and adaption to changing interface

Characteristics	Integrated circuit		
	FADIC	SIVIC	SAA2500
Function	Demodulation	Channel decoding	Audio decoding
Algorithm	FFT (2084 points)	Viterbi (64 states)	MPEG layer II
DAB modes	Mode I	Modes I, II, III	n/a
Design level	Behaviour	Register transfer	Register transfer
Technology	CMOS 1.0 micron	CMOS 0.8 micron	CMOS 0.8 micron
Size (mm^2)	>100	<50	<50
Package	CLCC–68	QFP–64	QFP–44
On–chip memory	DRAM 160 k	SRAM 14 k	SRAM
Off–chip memory	None	DRAM 256 k $\times$ 4	None
Data capacity	3 Mbyte/s	384 kbyte/s	384 kbyte/s
Processing unit	Symbol	Capacity unit (CU)	Frame
Control interface	16–bit DSP	L3/µC	L3/µC
Dissipation	500 mW	300 mW	100 mW

Table 3
Main characteristics of the ASICs developed by Philips for DAB.

formats without PCB modifications. The interfaces were designed in such a way that their direction could be reversed; by re–programming the DSPs and the GALs, it was possible to realise a partial channel encoder, which allows simple back–to–back verification and realisation of a test transmitter.

The decoder board is able to process the synchronization channel and one service component (4 symbols in Mode I, 16 in Mode II and 32 in Mode III). The maximum output bit–rate is 256 kbit/s.

The general–purpose approach proved to offer enough flexibility for the implementation of a system which was not yet fixed. The major design effort was expended on software rather than on hardware, especially for the implementation of Mode I with its distinct frame structure which took several

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In 1983 he joined N.V. Philips Industrial Activities where he was involved in the development of analogue ICs for audio applications. Since 1989 he has been working on DAB; he is involved in standardization issues and the realisation of DAB receivers, with special focus on control algorithms and their implementation.

Rob Olde Dubbelink *studied electrical engineering at the University of Twente in Enscede, in the Netherlands. He obtained his degree in 1990 and in 1991 joined the Advanced Development Centre of Philips Consumer Electronics. He is involved in simulation programs for channel decoder ASICs, the testing of DAB receivers and the delivery of DAB test systems.*

months of effort. Although the algorithms are quite complex, their implementation was relatively simple. More attention had to be given to proper interrupt handling, to ensure that data was not lost from memory–mapped I/O and serial interfaces. These complications are typical in real implementation and do not occur in simulation programs. It was discovered that the non–orthogonality of the DSP instruction set limited the effectiveness of both the design and execution time of the DSP algorithms. Reduced instruction sets and automatic context switching would have been more effective in real–time applications like these.

4.2. Design of an ASIC set

The DSP–based prototypes were built as a means of gaining a complete understanding of the system, for verification of the standard and to prove its viability by field tests. For an economic implementation in a car, however, a significant reduction in size, price and power consumption is needed. Therefore Philips Consumer Electronics has developed application–specific integrated circuits (ASIC) for the channel decoder and the audio decoder within the JESSI AE14 project. The partitioning of this chipset corresponds to the functional partitioning shown in *Fig. 5*. A summary of the main ASIC characteristics is given in *Table 3*. One DSP is reserved for synchronization tasks and display of the channel impulse response (CIR); this allows further optimization of the algorithms before integration.

With the DSP solution it was necessary to use the complete 24 ms frame duration for demodulation of one service component. With the ASIC solution the choice was made to do real–time processing on a symbol basis [12]. This offers the following advantages:

– Processing delay and buffer sizes are reduced from one frame to one symbol, at the expense of a more complex arithmetic unit.

– More regularity and thus simplified control.

– Demodulation of a complete ensemble is possible. Power dissipation will be reduced if only a sub–set of the symbols are selected for demodulation.

For the decoder part it is desirable to be able to process at least three service components simultaneously, for example FIC data (32 kbit/s), audio ($\leq$256 kbit/s) and other data ($\leq$64 kbit/s).

The total net data rate for the three channels corresponds to a requirement for a decoding capability of at least 352 kbit/s. Considering a 12.288–MHz system clock and a 64–state Viterbi decoder, an output data–rate of 384 kbit/s can be achieved by the sequential processing of two combined states in each clock cycle. For the time de–interleaving of one audio service plus a data service component, and frame buffering for all components, about 256k $\times$ 4 of RAM is needed. An external DRAM is used for this, with the controller integrated on the decoder. By carefully taking into account the frame structure, no refresh cycles are needed.

Figure 9
Impression of a DAB test and measurement receiver of the next generation.

All ASICs operate on a single 5V supply with a 12.288 MHz system clock. A boundary scan test (BST) is implemented for the testing of printed circuit board assembly. Recently a prototype receiver has been constructed based on these ICs. First results show that this receiver is working correctly for stationary reception in Mode I. The next development step is the design of a demodulation ASIC, which will support all DAB transmission modes. *Fig. 9* gives an impression of how a next generation of receiver might look.

4.3. Evaluation

A baseband simulation program was written before the hardware implementations took place. The program was used for building up system knowledge, for studying the effects of coding and interleaving on different channel characteristics and as a reference for implementation. The results of simulations in a Gaussian and a Rayleigh channel are given in *Fig. 10*, which shows the bit–error rate (BER) of a decoded sequence as a function of the signal–to–noise ratio E_b/N_o where E_b is the energy per received bit and N_o the variance of the noise. It clearly shows the effect of using interleaving in a Rayleigh channel.

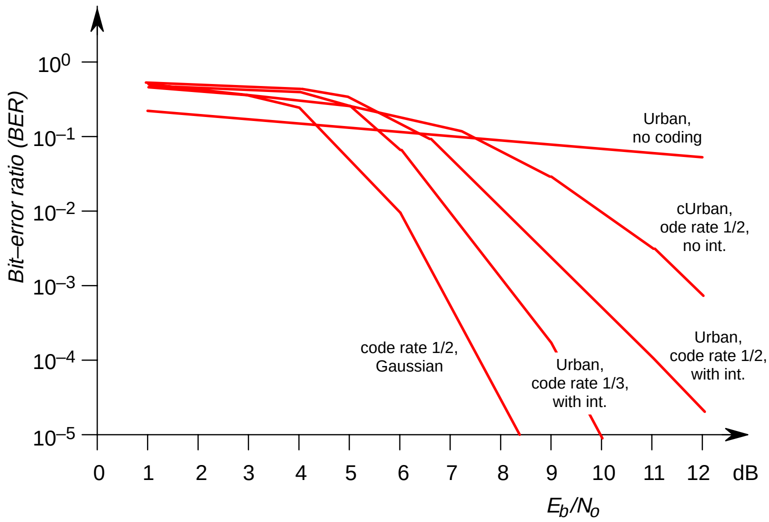

Figure 10
Simulated bit–error rate as a function of the signal–to–noise ratio E_b/N_o.

The curve for the Gaussian channel was compared with results of measurements on the DSP decoder, with a signal applied at the IF level and without using AFC. The carrier–to–noise ratio (C/N) was measured with a spectrum analyser and converted to a E_b/N_o value. The same IF oscillator was used for the transmitter and receiver. No significant differences were found between the simulations and the measurement results on the DSP decoder.

5. Conclusions

Prototype DAB receivers based upon DSPs and functioning according to the Eureka–147 standard are available and are being used world–wide for field tests, for measurement and for verification of the standard. They show the robustness of the Eureka–147 DAB system.

Prototype ASICs for channel decoding and audio decoding are also available now, and these will allow the construction of small size and reasonably–priced car–radio DAB receivers for the market introduction of DAB.

DSP/GAL design is very effective for making prototype decoders while the standardization process is under way. Although the design effort needed for an ASIC set is significant greater than for a DSP solution, it is impossible to make a feasible consumer product without it.

The chip size is mainly determined by the Mode I implementation, which took a lot of design effort for both DSP and ASIC approaches. From a receiver point of view, Modes II and III are more attractive for low–cost and small–size IC implementation.

Additional receiver design efforts should concentrate on price reduction of IF oscillators, the implementation of useful data services, the reduction of electromagnetic radiation to allow portable receivers to be offered, the use of a 3V power supply and combination with FM radio.

For the successful introduction of DAB it is also important that broadcasters and receiver manufacturers concur on the choice of same initial features, chosen from the numerous possibilities offered by the standard.

Acknowledgement

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